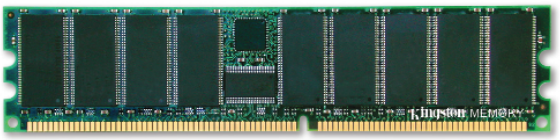
KINGSTON MEMORY

# SYSTEM MEMORY BY TECHNOLOGY



## THE DRAM EVOLUTION

Memory innovations like Synchronous DRAM (SDRAM), DDR, and Rambus™ have all contributed to finding a solution to the ever-increasing challenge of getting information to and from the processor more efficiently.

## DRAM (Dynamic Random Access Memory)

DRAM chips are designed as a matrix of "memory cells" laid down in rows and columns like squares on a checkerboard. Each memory cell is used to store bits of data which can be retrieved by indicating the row and column location (or address). The system uses DRAM to temporarily store information that moves to and from the processor, video card and peripherals. Older computers use **Fast Page Mode (FPM) DRAM.** This kind of memory was an improvement over earlier forms of DRAM because it accessed data on the same row or "page" faster. If the data required was on the same page as the previous data, the memory controller did not have to repeat the page location; it only needed to indicate the next column location.

## EDO DRAM

Extended Data Out (EDO) DRAM is similar to FPM, with a slight modification making back-to-back accessing of memory much faster. The primary advantage of EDO is that it keeps data available longer so it quickens sequential memory read operations. Performance gains over FPM are approximately 10 to 20 percent. EDO will continue to support servers and routers in limited capacities.

## SYNCHRONOUS DRAM (SDRAM)

Retrieval of information is synchronized with the system clock that controls the CPU. Being "in sync" with the processor eliminates timing chain delays and makes the memory retrieval process much more efficient. The memory cells inside the SDRAM chip are divided into multiple, independent "cell banks." Multiple banks can be activated simultaneously which provides a continuous flow of data by switching between banks. This method cuts down the total memory read cycle and results in faster transfer rates. SDRAM is available in 66MHz, 100MHz and 133MHz.

## DDR SDRAM

DDR (Double Data Rate) is the next generation of SDRAM. DDR finds its foundations on the same design core of SDRAM, yet advances its **speed** capabilities. DDR essentially doubles the memory **speed** from SDRAMs without increasing the clock frequency (DDR allows data to be read on both the rising and falling edge of the clock, delivering twice the bandwidth of standard SDRAMs). For example, a 200MHz DDR module will deliver 1.6GB per second memory bandwidth versus the 800MB per second that PC100 delivers. The DDR DIMM module changes as well, using a 184-pin count module with 2.5 volt memory chips. Motherboard and systems are specifically designed to support DDR memory. Therefore, DDR DIMMs cannot be used in a system supporting PC100 or PC133 DIMMs. DDR is currently available in 200MHz, 266MHz and 333MHz. Device=200, 266 and 333MHz. Module=PC1600, PC2100 and PC2700.

## RAMBUS

Direct Rambus is the third generation of Rambus. RDRAM uses the same signaling (RSL), but has a higher frequency (800MHz) and improved packet-based protocol. **A single Direct RDRAM Channel (16 bit) will deliver 1.6GB per second memory bandwidth.** RDRAM on a RIMM™ module can support up to four simultaneous transactions. The RSL technology permits the 800MHz transfer rates. Performance gains over SDRAM–100MHz systems are three times the peak bandwidth.

RIMM is the trademarked name for Rambus memory modules. RIMM modules utilize a 184-pin module with 2.5 volt memory chips. The system boards support two RIMM connectors with a maximum of 32 RDRAM chips per channel. Rambus requires that all connectors be filled to allow the flow-through of key signals. Because of this, a Continuity RIMM is used in connectors not populated with a RIMM.



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